IN THE CLAIMS:

Claims 1 through 30 and 36 were previously cancelled. Claims 35 and 42 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1.-30. (Cancelled)

31. (Previously presented) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of mesas comprising a plurality of contiguous top surfaces, the mesas forming a maze-like structure.

32. (Previously presented) The storage poly of claim 31, wherein the mesas extend in the X, Y and Z coordinates.

33. (Previously presented) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of webs comprising a plurality of contiguous top surfaces, the webs forming a maze-like structure; and
hemispherical-grain polysilicon on at least some of the plurality of contiguous top surfaces.

34. (Previously presented) The storage poly of claim 33, wherein the webs extend in the X, Y and Z coordinates.

35. (Currently amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure comprising a plurality of mesas with recesses therebetween;

a contiguous hemispherical-grain polysilicon layer forming a maze-like structure on the storage poly structure and in contact therewith; and

a mask over the contiguous hemispherical-grain polysilicon layer, the recesses being exposed through the contiguous hemispherical-grain polysilicon layer and the mask.

36. (Cancelled)

37. (Previously presented) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure;

a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer forming a maze-like structure on the storage poly structure;

recesses formed in the storage poly structure and located laterally between the plurality of contiguous low elevation regions of the hemispherical-grain polysilicon layer; and

dielectric material at least lining the recesses.

38. (Previously presented) A semiconductor memory cell structure, comprising:
a storage poly structure;
regions of hemispherical-grain polysilicon on at least portions of an upper surface of the storage poly structure;
a plurality of recesses extending into the storage poly structure, at least some recesses of the plurality of recesses being located laterally between the regions of hemispherical-grain polysilicon and imparting the storage poly structure with a structure resembling a plurality of mesas, top surfaces of the plurality of mesas forming a maze-like structure; and
a dielectric layer coating an upper surface of the storage poly structure and lining each of the plurality of recesses.

39. (Previously presented) The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over the dielectric layer.

40. (Previously presented) The semiconductor memory cell structure of claim 38, wherein the regions of hemispherical-grain polysilicon have a web-like appearance.

41. (Previously presented) The semiconductor memory cell structure of claim 38, wherein at least some of the plurality of recesses extend into the storage poly structure.

42. (Currently amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure;
a confluent hemispherical-grain polysilicon layer on the storage poly structure; and
a mask forming a maze-like structure positioned over the confluent hemispherical-grain polysilicon layer, planarized portions of the confluent hemispherical-grain polysilicon layer being exposed through the mask.

43. (Previously presented) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses therein;

remaining portions of a hemispherical-grain polysilicon layer forming a maze-like structure overlying upper portions of the storage poly structure; and

a mask positioned over the hemispherical-grain polysilicon layer and spaced apart from the storage poly structure by the remaining portions of the hemispherical-grain polysilicon layer, the recesses in the storage poly structure being exposed through the mask.

44. (Previously presented) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses therein;

a hemispherical-grain polysilicon layer forming a maze-like structure on at least portions of the storage poly structure; and

dielectric material lining at least the recesses.

45. (Previously presented) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure with recesses therein;

low elevation regions of a hemispherical-grain polysilicon layer forming a maze-like structure on at least portions of the storage poly structure; and

dielectric material at least lining the recesses.